60 MHz, 2000 V/μs Monolithic Op Amp

AD844

FEATURES

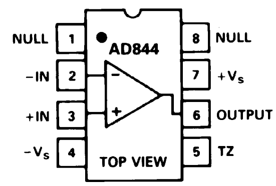
Wide Bandwidth: 60 MHz at Gain of –1
33 MHz at Gain of –10
Very High Output Slew Rate: Up to 2000 V/μs
20 MHz Full Power Bandwidth, 20 V pk-pk, R_L = 500 Ω
Fast Settling: 100 ns to 0.1% (10 V Step)
Differential Gain Error: 0.03% at 4.4 MHz
Differential Phase Error: 0.15° at 4.4 MHz
High Output Drive: ±50 mA into 50 Ω Load
Low Offset Voltage: 150 μV max (B Grade)
Low Quiescent Current: 6.5 mA
Available in Tape and Reel in Accordance with EIA-481A Standard

APPLICATIONS

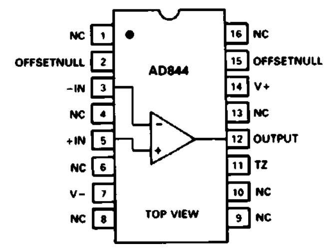
Flash ADC Input Amplifiers
High Speed Current DAC Interfaces
Video Buffers and Cable Drivers
Pulse Amplifiers

CONNECTION DIAGRAMS

8-Pin Plastic (N), and Cerdip (Q) Packages



16-Pin SOIC (R) Package



PRODUCT DESCRIPTION

The AD844 is a high speed monolithic operational amplifier fabricated using Analog Devices' junction isolated complementary bipolar (CB) process. It combines high bandwidth and very fast large signal response with excellent dc performance. Although optimized for use in current to voltage applications and as an inverting mode amplifier, it is also suitable for use in many non-inverting applications.

The AD844 can be used in place of traditional op amps, but its current feedback architecture results in much better ac performance, high linearity and an exceptionally clean pulse response.

This type of op amp provides a closed-loop bandwidth which is determined primarily by the feedback resistor and is almost independent of the closed-loop gain. The AD844 is free from the slew rate limitations inherent in traditional op amps and other current-feedback op amps. Peak output rate of change can be over 2000 V/μs for a full 20 V output step. Settling time is typically 100 ns to 0.1%, and essentially independent of gain. The AD844 can drive 50 Ω loads to ±2.5 V with low distortion and is short circuit protected to 80 mA.

The AD844 is available in four performance grades and three package options. In the 16-pin SOIC (R) package, the AD844J is specified for the commercial temperature range of 0°C to +70°C. The AD844A and AD844B are specified for the industrial temperature range of –40°C to +85°C and are available in the cerdip (Q) package. The AD844A is also available in an 8-pin plastic mini-DIP (N). The AD844S is specified over the military temperature range of –55°C to +125°C. It is available in the 8-pin cerdip (Q) package. "A" and "S" grade chips and devices processed to MIL-STD-883B, REV. C are also available.

PRODUCT HIGHLIGHTS

1. The AD844 is a versatile, low cost component providing an excellent combination of ac and dc performance. It may be used as an alternative to the EL2020 and CLC400/1.
2. It is essentially free from slew rate limitations. Rise and fall times are essentially independent of output level.
3. The AD844 can be operated from ±4.5 V to ±18 V power supplies and is capable of driving loads down to 50 Ω, as well as driving very large capacitive loads using an external network.
4. The offset voltage and input bias currents of the AD844 are laser trimmed to minimize dc errors; V_{OS} drift is typically 1 μV/°C and bias current drift is typically 9 nA/°C.
5. The AD844 exhibits excellent differential gain and differential phase characteristics, making it suitable for a variety of video applications with bandwidths up to 60 MHz.
6. The AD844 combines low distortion, low noise and low drift with wide bandwidth, making it outstanding as an input amplifier for flash A/D converters.

REV. C

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 617/329-4700 Fax: 617/326-8703

AD844–SPECIFICATIONS (@ T_A = +25°C and V_S = ±15 V dc, unless otherwise noted)

Model	Conditions	AD844J/A			AD844B			AD844S			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
INPUT OFFSET VOLTAGE[1]			50	**300**		50	**150**		50	**300**	µV
T_{MIN}–T_{MAX}			75	500		75	**200**		125	**500**	µV
vs. Temperature			1			1	5		1	5	µV/°C
vs. Supply	5 V–18 V										
Initial			4	**20**		4	**10**		4	**20**	µV/V
T_{MIN}–T_{MAX}			4			4	**10**		4	**20**	µV/V
vs. Common Mode	V_{CM} = ±10 V										
Initial			10	**35**		10	**20**		10	**35**	µV/V
T_{MIN}–T_{MAX}			10			10	**20**		10	**35**	µV/V
INPUT BIAS CURRENT											
–Input Bias Current[1]			200	**450**		150	**250**		200	**450**	nA
T_{MIN}–T_{MAX}			800	1500		750	**1100**		1900	**2500**	nA
vs. Temperature			9			9	15		20	30	nA/°C
vs. Supply	5 V–18 V										
Initial			175	**250**		**175**	**200**		175	**250**	nA/V
T_{MIN}–T_{MAX}			220			220	**240**		220	**300**	nA/V
vs. Common Mode	V_{CM} = ±10 V										
Initial			90	**160**		90	**110**		90	**160**	nA/V
T_{MIN}–T_{MAX}			110			110	**150**		120	**200**	nA/V
+Input Bias Current[1]			150	**400**		100	**200**		100	**400**	nA
T_{MIN}–T_{MAX}			350	700		300	**500**		800	**1300**	nA
vs. Temperature			3			3	7		7	15	nA/°C
vs. Supply	5 V–18 V										
Initial			80	**150**		80	**100**		80	**150**	nA/V
T_{MIN}–T_{MAX}			100			100	**120**		120	**200**	nA/V
vs. Common Mode	V_{CM} = ±10 V										
Initial			90	**150**		90	**120**		**90**	**150**	nA/V
T_{MIN}–T_{MAX}			130			130	**190**		**140**	**200**	nA/V
INPUT CHARACTERISTICS											
Input Resistance											
–Input			50	65		50	65		50	65	Ω
+Input		7	10		7	10		7	10		MΩ
Input Capacitance											
–Input			2			2			2		pF
+Input			2			2			2		pF
Input Voltage Range											
Common Mode		±10			±10			±10			V
INPUT VOLTAGE NOISE	f ≥ 1 kHz		2			2			2		nV/√Hz
INPUT CURRENT NOISE											
–Input	f ≥ 1 kHz		10			10			10		pA/√Hz
+Input	f ≥ 1 kHz		12			12			12		pA/√Hz
OPEN LOOP TRANSRESISTANCE	V_{OUT} = ±10 V										
	R_{LOAD} = 500 Ω	**2.2**	3.0		**2.8**	3.0		**2.2**	3.0		MΩ
T_{MIN}–T_{MAX}		1.3	2.0		**1.6**	2.0		**1.3**	1.6		MΩ
Transcapacitance			4.5			4.5			4.5		pF
DIFFERENTIAL GAIN ERROR[2]	f = 4.4 MHz		0.03			0.03			0.03		%
DIFFERENTIAL PHASE ERROR[2]	f = 4.4 MHz		0.15			0.15			0.15		Degree
FREQUENCY RESPONSE											
Small Signal Bandwidth											
[3]Gain = –1			60			60			60		MHz
[4]Gain = –10			33			33			33		MHz
TOTAL HARMONIC DISTORTION	f = 100 kHz, 2 V rms[5]		0.005			0.005			0.005		%
SETTLING TIME											
10 V Output Step	±15 V Supplies										
Gain = –1, to 0.1%[5]			100			100			100		ns
Gain = –10, to 0.1%[6]			100			100			100		ns
2 V Output Step	±5 V Supplies										
Gain = –1, to 0.1%[5]			110			110			110		ns
Gain = –10, to 0.1%[6]			100			100			100		ns

Model	Conditions	AD844J/A Min	AD844J/A Typ	AD844J/A Max	AD844B Min	AD844B Typ	AD844B Max	AD844S Min	AD844S Typ	AD844S Max	Units
OUTPUT SLEW RATE	Overdriven Input	1200	2000		1200	2000		1200	2000		V/µs
FULL POWER BANDWIDTH											
V_{OUT} = 20 V p-p[5]	V_S = ±15 V		20			20			20		MHz
V_{OUT} = 2 V p-p[5]	V_S = ±5 V THD = 3%		20			20			20		MHz
OUTPUT CHARACTERISTICS											
Voltage	R_{LOAD} = 500 Ω	**10**	11		**10**	11		**10**	11		±V
Short Circuit Current			80			80			80		mA
T_{MIN}–T_{MAX}			60			60			60		mA
Output Resistance	Open Loop		15			15			15		Ω
POWER SUPPLY											
Operating Range		±4.5		±18	±4.5		±18	+4.5		±18	V
Quiescent Current			6.5	7.5		6.5	7.5		6.5	7.5	mA
T_{MIN}–T_{MAX}			7.5	8.5		7.5	8.5		8.5	9.5	mA

NOTES
[1]Rated performance after a 5 minute warmup at T_A = 25°C.
[2]Input signal 285 mV p-p carrier (40 IRE) riding on 0 mV to 642 mV (90 IRE) ramp. R_L= 100 Ω; R1, R2 = 300 Ω.
[3]Input signal 0 dBm, C_L = 10 pF, R_L = 500 Ω, R1 = 500 Ω, R2 = 500 Ω in Figure 26.
[4]Input signal 0 dBm, C_L =10 pF, R_L = 500 Ω, R1 = 500 Ω, R2 = 50 Ω in Figure 26.
[5]C_L = 10 pF, R_L = 500 Ω, R1 = 1 kΩ, R2 = 1 kΩ in Figure 26.
[6]C_L = 10 pF, R_L = 500 Ω, R1 = 500 Ω, R2 = 50 Ω in Figure 26.

Specifications subject to change without notice. All min and max specifications are guaranteed.
Specifications shown in **boldface** are tested on all production units at final electrical test.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . ±18 V
Power Dissipation[2] . . . . 1.1 W
Output Short Circuit Duration . . . . Indefinite
Common-Mode Input Voltage . . . . $\pm V_S$
Differential Input Voltage . . . . 6 V
Inverting Input Current
  Continuous . . . . 5 mA
  Transient . . . . 10 mA
Storage Temperature Range (Q) . . . . –65°C to +150°C
  (N, R) . . . . –65°C to +125°C
Lead Temperature Range (Soldering 60 sec) . . . . +300°C
ESD Rating . . . . 1000 V

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]28-Pin Plastic Package: θ_{JA} = 100°C/Watt
8-Pin Cerdip Package: θ_{JA} = 110°C/Watt
16-Pin SOIC Package: θ_{JA} = 100°C/Watt

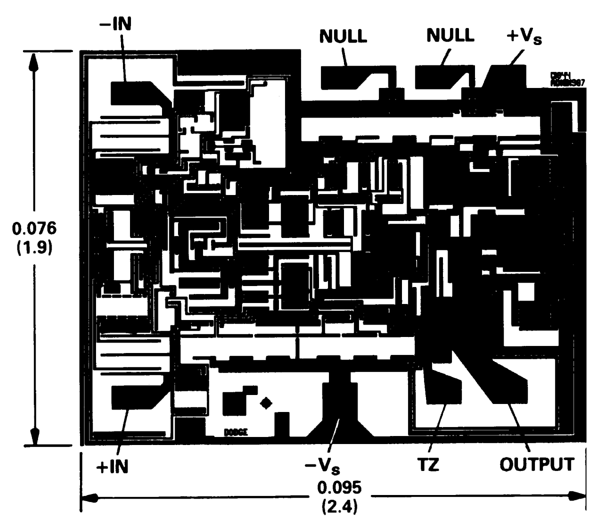
ORDERING GUIDE

Model	Temperature Range	Package Option*
AD844JR	0°C to +70°C	R-16
AD844JR-REEL	0°C to +70°C	Tape and Reel
AD844AN	–40°C to +85°C	N-8
AD844AQ	–40°C to +85°C	Q-8
AD844BQ	–40°C to +85°C	Q-8
AD844SQ	–55°C to +125°C	Q-8
AD844SQ/883B	–55°C to +125°C	Q-8
5962-8964401PA	–55°C to +125°C	Q-8
AD844A Chips	–40°C to +85°C	Die
AD844S Chips	–55°C to +125°C	Die

*N = Plastic DIP; Q = Cerdip; R = Small Outline IC (SOIC).

METALIZATION PHOTOGRAPH

Contact factory for latest dimensions.
Dimension shown in inches and (mm).



SUBTRATE CONNECTED TO $+V_S$

AD844–Typical Characteristics (T_A = +25°C and V_S = ±15 V, unless otherwise noted)

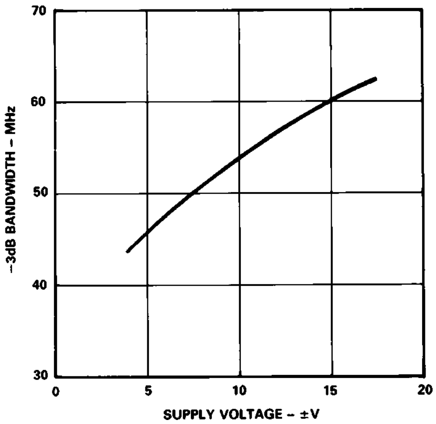


Figure 1. –3 dB Bandwidth vs. Supply Voltage R1 = R2 = 500 Ω

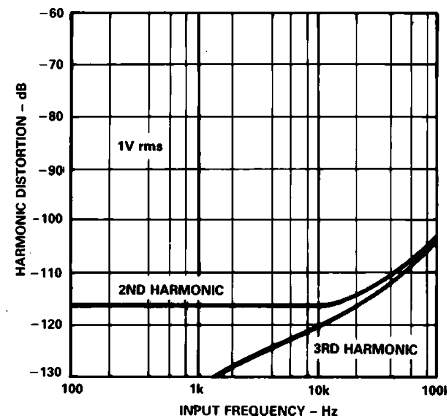


Figure 2. Harmonic Distortion vs. Frequency, R1 = R2 = 1 kΩ

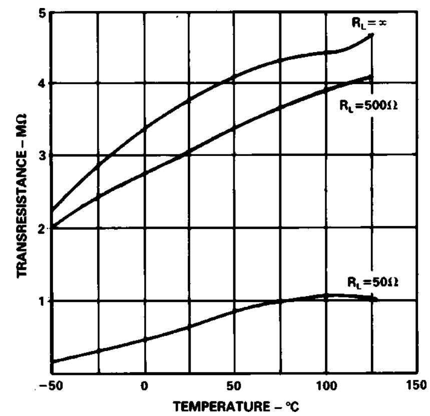


Figure 3. Transresistance vs. Temperature

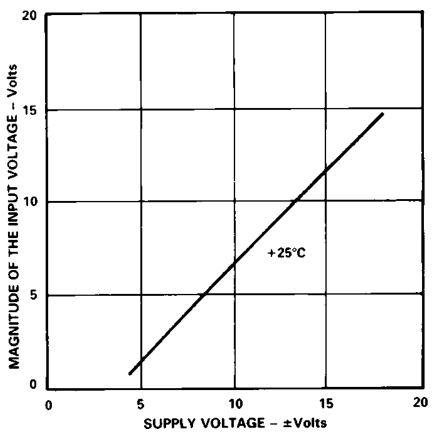


Figure 4. Noninverting Input Voltage Swing vs. Supply Voltage

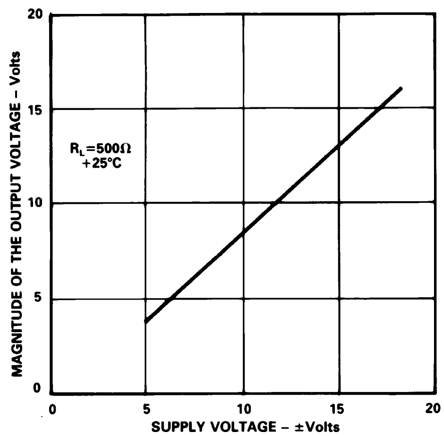


Figure 5. Output Voltage Swing vs. Supply Voltage

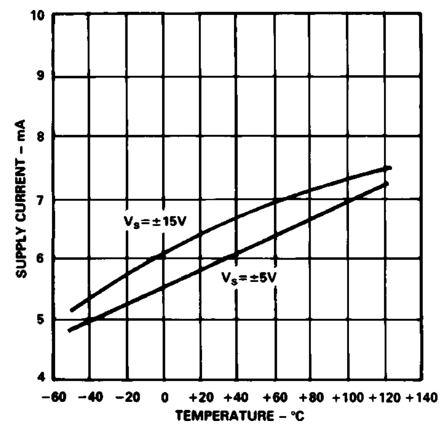


Figure 6. Quiescent Supply Current vs. Temperature and Supply Voltage

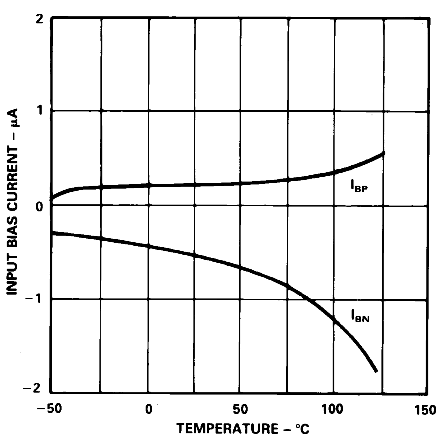


Figure 7. Inverting Input Bias Current (I_{BN}) and Noninverting Input Bias Current (I_{BP}) vs. Temperature

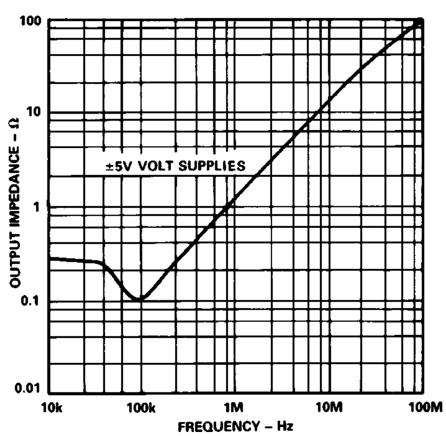


Figure 8. Output Impedance vs. Frequency, Gain = –1, R1 = R2 = 1 kΩ

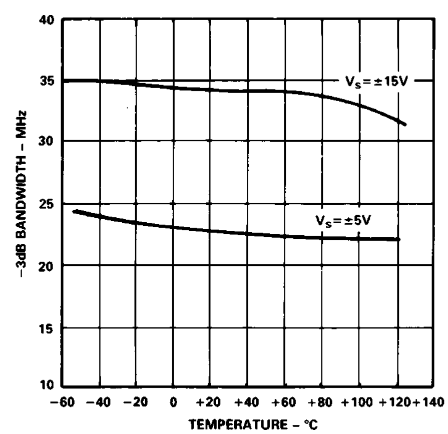


Figure 9. –3 dB Bandwidth vs. Temperature, Gain = –1, R1 = R2 = 1 kΩ

Inverting Gain of 1 AC Characteristics

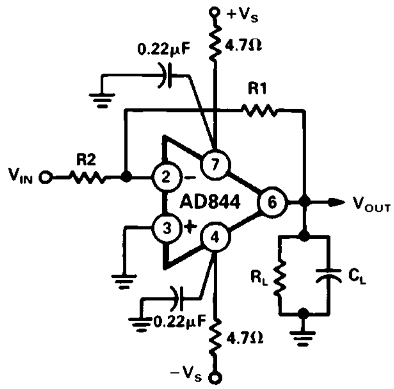


Figure 10. Inverting Amplifier, Gain of –1 (R1 = R2)

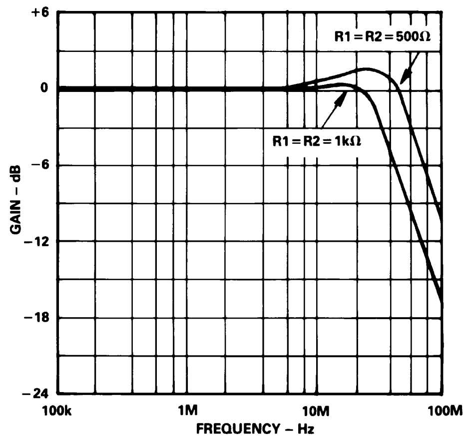


Figure 11. Gain vs. Frequency for Gain = –1, R_L = 500 Ω, C_L = 0 pF

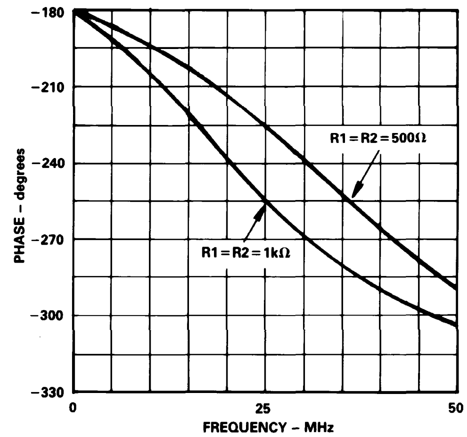


Figure 12. Phase vs. Frequency Gain = –1, R_L = 500 Ω, C_L = 0 pF

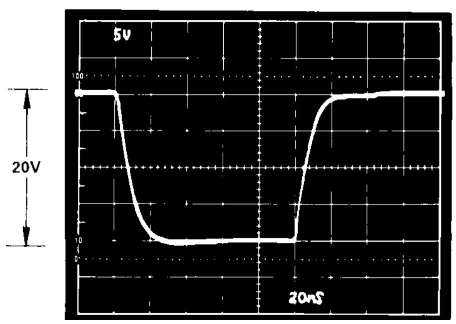


Figure 13. Large Signal Pulse Response, Gain = –1, R1 = R2 = 1 kΩ

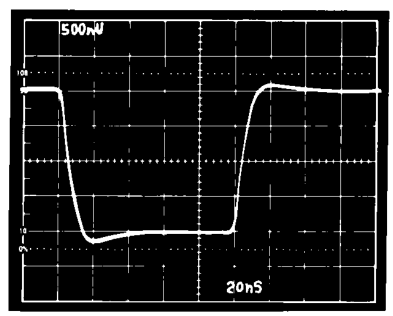


Figure 14. Small Signal Pulse Response, Gain = –1, R1 = R2 = 1 kΩ

Inverting Gain of 10 AC Characteristics

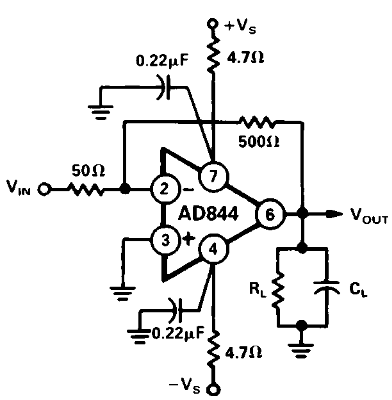


Figure 15. Gain of –10 Amplifier

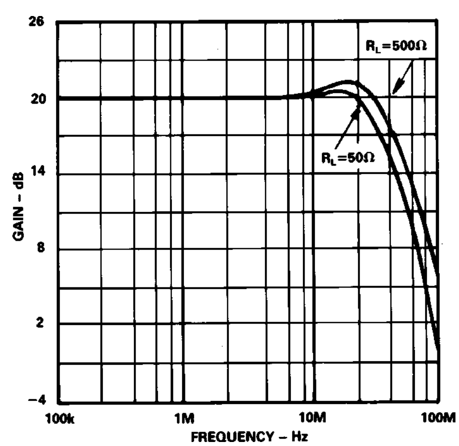


Figure 16. Gain vs. Frequency, Gain = –10

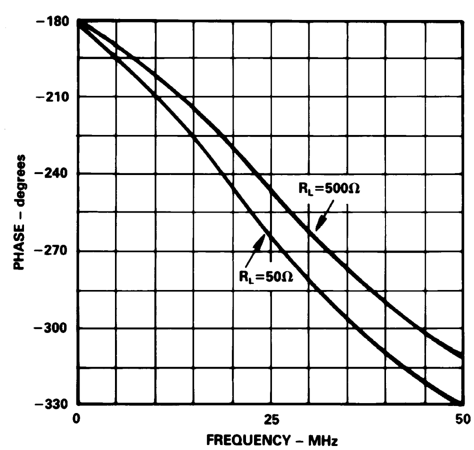


Figure 17. Phase vs. Frequency, Gain = –10

Inverting Gain of 10 Pulse Response

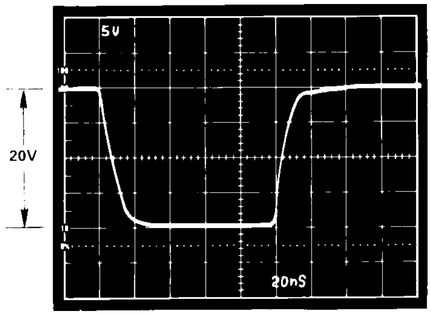


Figure 18. Large Signal Pulse Response, Gain = –10, R_L = 500 Ω

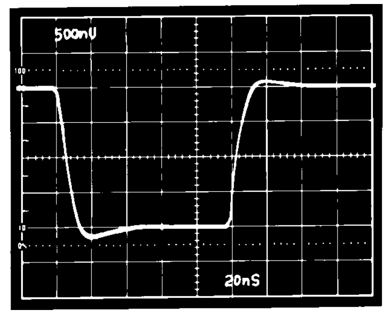


Figure 19. Small Signal Pulse Response, Gain = –10, R_L = 500 Ω

Noninverting Gain of 10 AC Characteristics

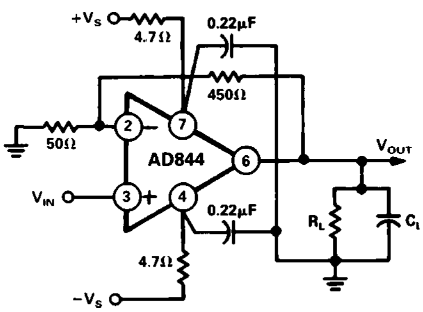


Figure 20. Noninverting Gain of +10 Amplifier

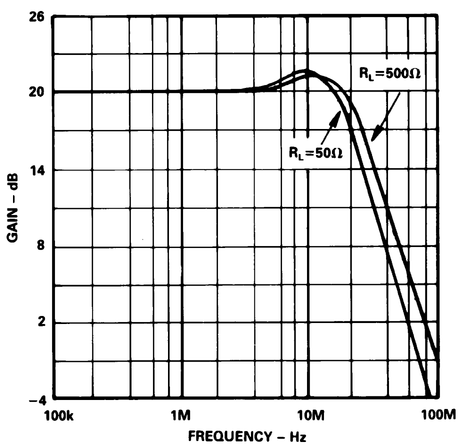


Figure 21. Gain vs. Frequency, Gain = +10

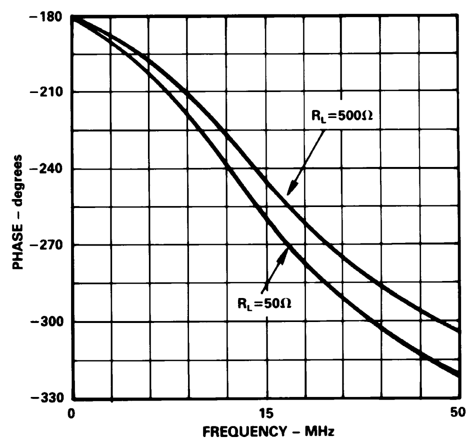


Figure 22. Phase vs. Frequency, Gain = +10

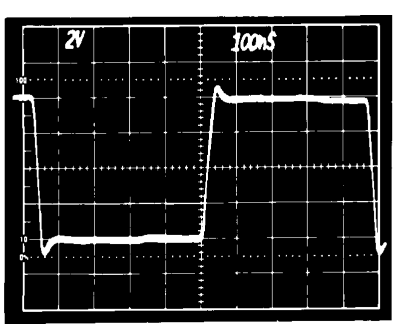


Figure 23. Noninverting Amplifier Large Signal Pulse Response, Gain = +10, R_L = 500 Ω

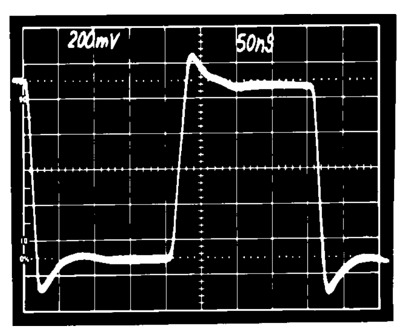


Figure 24. Small Signal Pulse Response, Gain = +10, R_L = 500 Ω

UNDERSTANDING THE AD844

The AD844 can be used in ways similar to a conventional op amp while providing performance advantages in wideband applications. However, there are important differences in the internal structure which need to be understood in order to optimize the performance of the AD844 op amp.

Open Loop Behavior

Figure 25 shows a current feedback amplifier reduced to essentials. Sources of fixed dc errors such as the inverting node bias current and the offset voltage are excluded from this model and are discussed later. The most important parameter limiting the dc gain is the transresistance, Rt, which is ideally infinite. A finite value of Rt is analogous to the finite open loop voltage gain in a conventional op amp.

The current applied to the inverting input node is replicated by the current conveyor so as to flow in resistor Rt. The voltage developed across Rt is buffered by the unity gain voltage follower. Voltage gain is the ratio Rt/ R_{IN}. With typical values of Rt = 3 MΩ and R_{IN} = 50 Ω, the voltage gain is about 60,000. The open loop current gain is another measure of gain and is determined by the beta product of the transistors in the voltage follower stage (see Figure 28); it is typically 40,000.

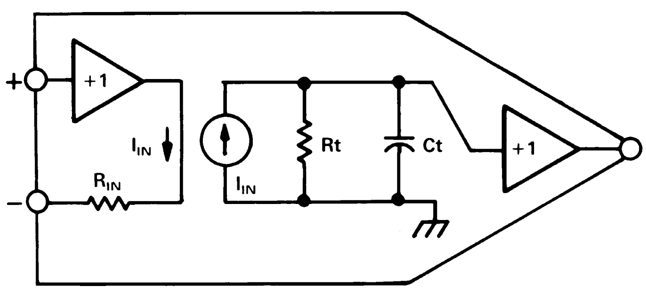


Figure 25. Equivalent Schematic

The important parameters defining ac behavior are the transcapacitance, Ct, and the external feedback resistor (not shown). The time constant formed by these components is analogous to the dominant pole of a conventional op amp, and thus cannot be reduced below a critical value if the closed loop system is to be stable. In practice, Ct is held to as low a value as possible (typically 4.5 pF) so that the feedback resistor can be maximized while maintaining a fast response. The finite R_{IN} also affects the closed loop response in some applications as will be shown.

The open loop ac gain is also best understood in terms of the transimpedance rather than as an open loop voltage gain. The open loop pole is formed by Rt in parallel with Ct. Since Ct is typically 4.5 pF, the open loop corner frequency occurs at about 12 kHz. However, this parameter is of little value in determining the closed loop response.

Response as an Inverting Amplifier

Figure 26 shows the connections for an inverting amplifier. Unlike a conventional amplifier the transient response and the small signal bandwidth are determined primarily by the value of the external feedback resistor, R1, rather than by the ratio of R1/R2 as is customarily the case in an op amp application. This is a direct result of the low impedance at the inverting input. As with conventional op amps, the closed loop gain is –R1/R2.

The closed loop transresistance is simply the parallel sum of R1 and Rt. Since R1 will generally be in the range 500 Ω to 2 kΩ and Rt is about 3 MΩ the closed loop transresistance will be only 0.02% to 0.07% lower than R1. This small error will often be less than the resistor tolerance.

When R1 is fairly large (above 5 kΩ) but still much less than Rt, the closed loop HF response is dominated by the time constant R1Ct. Under such conditions the AD844 is over-damped and will provide only a fraction of its bandwidth potential. Because of the absence of slew rate limitations under these conditions, the circuit will exhibit a simple single pole response even under large signal conditions.

In Figure 26, R3 is used to properly terminate the input if desired. R3 in parallel with R2 gives the terminated resistance. As R1 is lowered, the signal bandwidth increases, but the time constant R1Ct becomes comparable to higher order poles in the closed loop response. Therefore, the closed loop response becomes complex, and the pulse response shows overshoot. When R2 is much larger than the input resistance, R_{IN}, at Pin 2, most of the feedback current in R1 is delivered to this input; but as R2 becomes comparable to R_{IN}, less of the feedback is absorbed at Pin 2, resulting in a more heavily damped response. Consequently, for low values of R2 it is possible to lower R1 without causing instability in the closed loop response. Table I lists combinations of R1 and R2 and the resulting frequency response for the circuit of Figure 26. Figure 13 shows the very clean and fast ±10 V pulse response of the AD844.

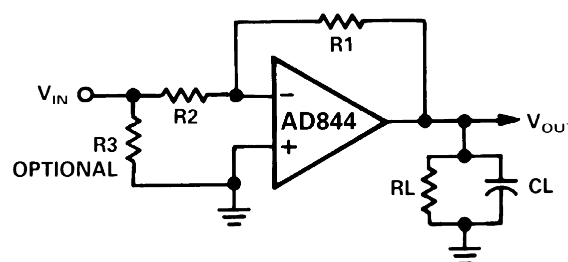


Figure 26. Inverting Amplifier

Table I.

Gain	R1	R2	BW (MHz)	GBW (MHz)
–1	1 kΩ	1 kΩ	35	35
–1	500 Ω	500 Ω	60	60
–2	2 kΩ	1 kΩ	15	30
–2	1 kΩ	500 Ω	30	60
–5	5 kΩ	1 kΩ	5.2	26
–5	500 Ω	100 Ω	49	245
–10	1 kΩ	100 Ω	23	230
–10	500 Ω	50 Ω	33	330
–20	1 kΩ	50 Ω	21	420
–100	5 kΩ	50 Ω	3.2	320
+100	5 kΩ	50 Ω	9	900

Response as an I-V Converter

The AD844 works well as the active element in an operational current to voltage converter, used in conjunction with an external scaling resistor, R1, in Figure 27. This analysis includes the stray capacitance, C_S, of the current source, which might be a high speed DAC. Using a conventional op amp, this capacitance forms a "nuisance pole" with R1 which destabilizes the closed loop response of the system. Most op amps are internally compensated for the fastest response at unity gain, so the pole due to R1 and C_S reduces the already narrow phase margin of the system. For example, if R1 were 2.5 kΩ a C_S of 15 pF would place this pole at a frequency of about 4 MHz, well within the response range of even a medium speed operational amplifier. In a current feedback amp this nuisance pole is no longer determined by R1 but by the input resistance, R_{IN}. Since this is about 50 Ω for the AD844, the same 15 pF forms a pole 212 MHz and causes little trouble. It can be shown that the response of this system is:

$$V_{OUT} = -Isig \frac{K\,R1}{(1+sTd)(1+sTn)}$$

where K is a factor very close to unity and represents the finite dc gain of the amplifier, Td is the dominant pole and Tn is the nuisance pole:

$$K = \frac{Rt}{Rt + R1}$$

$$Td = KR1Ct$$

$$Tn = R_{IN}C_S \qquad (assuming\ R_{IN} << R1)$$

Using typical values of R1 = 1 kΩ and Rt = 3 MΩ, K is 0.9997; in other words, the "gain error" is only 0.03%. This is much less than the scaling error of virtually all DACs and can be absorbed, if necessary, by the trim needed in a precise system.

In the AD844, Rt is fairly stable with temperature and supply voltages, and consequently the effect of finite "gain" is negligible unless high value feedback resistors are used. Since that would result in slower response times than are possible, the relatively low value of Rt in the AD844 will rarely be a significant source of error.

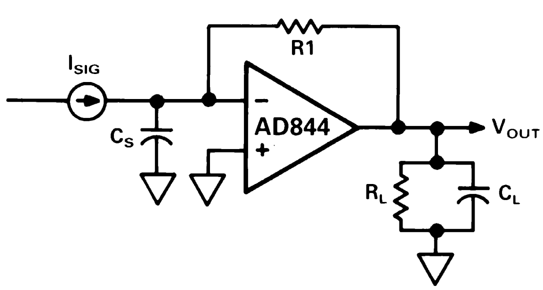


Figure 27. Current to Voltage Converter

Circuit Description of the AD844

A simplified schematic is shown in Figure 28. The AD844 differs from a conventional op amp in that the signal inputs have radically different impedance. The noninverting input (Pin 3) presents the usual high impedance. The voltage on this input is transferred to the inverting input (Pin 2) with a low offset voltage, ensured by the close matching of like polarity transistors operating under essentially identical bias conditions. Laser trimming nulls the residual offset voltage, down to a few tens of microvolts. The inverting input is the common emitter node of a complementary pair of grounded base stages and behaves as a current summing node. In an ideal current feedback op amp the input resistance would be zero. In the AD844 it is about 50 Ω.

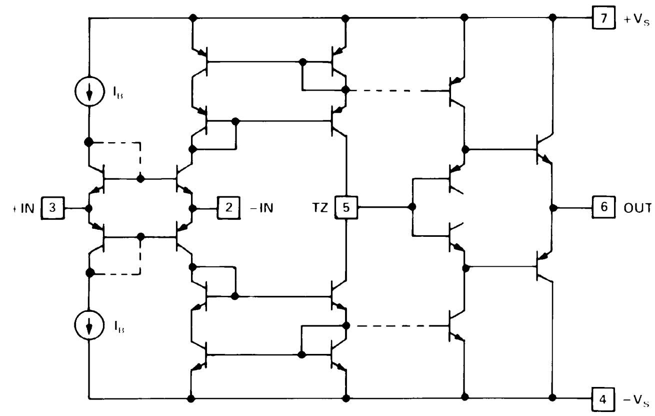


Figure 28. Simplified Schematic

A current applied to the inverting input is transferred to a complementary pair of unity-gain current mirrors which deliver the same current to an internal node (Pin 5) at which the full output voltage is generated. The unity-gain complementary voltage follower then buffers this voltage and provides the load driving power. This buffer is designed to drive low impedance loads such as terminated cables, and can deliver ±50 mA into a 50 Ω load while maintaining low distortion, even when operating at supply voltages of only ±6 V. Current limiting (not shown) ensures safe operation under short circuited conditions.

It is important to understand that the low input impedance at the inverting input is locally generated, and does not depend on feedback. This is very different from the "virtual ground" of a conventional operational amplifier used in the current summing mode which is essentially an open circuit until the loop settles. In the AD844, transient current at the input does not cause voltage spikes at the summing node while the amplifier is settling. Furthermore, all of the transient current is delivered to the slewing (TZ) node (Pin 5) via a short signal path (the grounded base stages and the wideband current mirrors).

The current available to charge the capacitance (about 4.5 pF) at TZ node, is *always proportional to the input error current,* and the slew rate limitations associated with the large signal response of op amps do not occur. For this reason, the rise and fall times are almost independent of signal level. In practice, the input current will eventually cause the mirrors to saturate. When using ±15 V supplies, this occurs at about 10 mA (or ±2200 V/µs). Since signal currents are rarely this large, classical "slew rate" limitations are absent.

This inherent advantage would be lost if the voltage follower used to buffer the output were to have slew rate limitations. The AD844 has been designed to avoid this problem, and as a result the output buffer exhibits a clean large signal transient response, free from anomalous effects arising from internal saturation.

Response as a Noninverting Amplifier

Since current feedback amplifiers are asymmetrical with regard to their two inputs, performance will differ markedly in noninverting and inverting modes. In noninverting modes, the large signal high speed behavior of the AD844 deteriorates at low gains because the biasing circuitry for the input system (not shown in Figure 28) is not designed to provide high input voltage slew rates.

However, good results can be obtained with some care. The noninverting input will not tolerate a large transient input; it must be kept below ±1 V for best results. Consequently this mode is better suited to high gain applications (greater than ×10). Figure 20 shows a noninverting amplifier with a gain of 10 and a bandwidth of 30 MHz. The transient response is shown in Figures 23 and 24. To increase the bandwidth at higher gains, a capacitor can be added across R2 whose value is approximately the ratio of R1 and R2 times Ct.

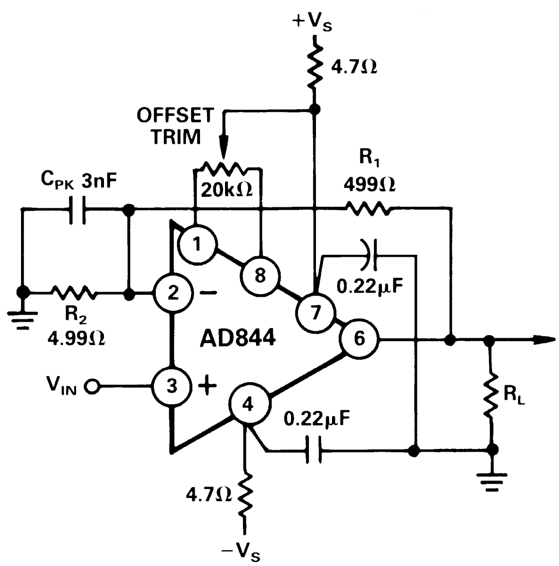


Figure 29. Noninverting Amplifier Gain = 100, Optional Offset Trim Is Shown

Noninverting Gain of 100

The AD844 provides very clean pulse response at high noninverting gains. Figure 29 shows a typical configuration providing a gain of 100 with high input resistance. The feedback resistor is kept as low as practicable to maximize bandwidth, and a peaking capacitor (C_{PK}) can optionally be added to further extend the bandwidth. Figure 30 shows the small signal response with C_{PK} = 3 nF, R_L = 500 Ω and supply voltages of either ±5 V or ±15 V. *Gain bandwidth products of up to 900 MHz can be achieved in this way.*

The offset voltage of the AD844 is laser trimmed to the 50 µV level and exhibits very low drift. In practice, there is an additional offset term due to the bias current at the inverting input (I_{BN}) which flows in the feedback resistor (R1). This can optionally be nulled by the trimming potentiometer shown in Figure 29.

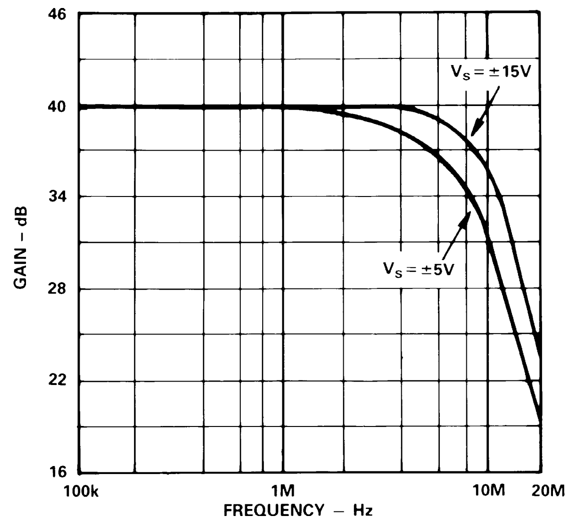


Figure 30. AC Response for Gain = 100, Configuration Shown in Figure 29

USING THE AD844

Board Layout

As with all high frequency circuits considerable care must be used in the layout of the components surrounding the AD844. A ground plane, to which the power supply decoupling capacitors are connected by the shortest possible leads, is essential to achieving clean pulse response. Even a continuous ground plane will exhibit finite voltage drops between points on the plane, and this must be kept in mind in selecting the grounding points. Generally speaking, decoupling capacitors should be taken to a point close to the load (or output connector) since the load currents flow in these capacitors at high frequencies. The +In and –In circuits (for example, a termination resistor and Pin 3) must be taken to a common point on the ground plane close to the amplifier package.

Use low impedance capacitors (AVX SR305C224KAA or equivalent) of 0.22 µF wherever ac coupling is required. Include either ferrite beads and/or a small series resistance (approximately 4.7 Ω) in each supply line.

Input Impedance

At low frequencies, negative feedback keeps the resistance at the inverting input close to zero. As the frequency increases, the impedance looking into this input will increase from near zero to the open loop input resistance, due to bandwidth limitations, making the input seem inductive. If it is desired to keep the input impedance flatter, a series RC network can be inserted across the input. The resistor is chosen so that the parallel sum of it and R2 equals the desired termination resistance. The capacitance is set so that the pole determined by this RC network is about half the bandwidth of the op amp. This network is not important if the input resistor is much larger than the termination used, or if frequencies are relatively low. In some cases, the small peaking that occurs without the network can be of use in extending the –3 dB bandwidth.

Driving Large Capacitive Loads

Capacitive drive capability is 100 pF without an external network. With the addition of the network shown in Figure 31, the capacitive drive can be extended to over 10,000 pF, limited by internal power dissipation. With capacitive loads, the output speed becomes a function of the overdriven output current limit. Since this is roughly ±100 mA, under these conditions, the maximum slew rate into a 1000 pF load is ±100 V/µs. Figure 32 shows the transient response of an inverting amplifier (R1 = R2 = 1 kΩ) using the feed forward network shown in Figure 31, driving a load of 1000 pF.

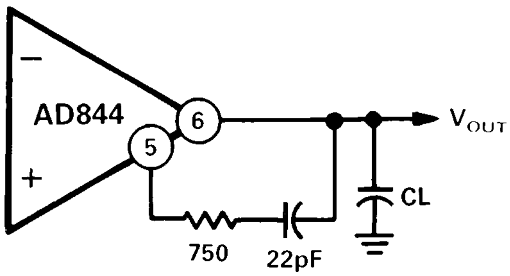


Figure 31. Feed Forward Network for Large Capacitive Loads

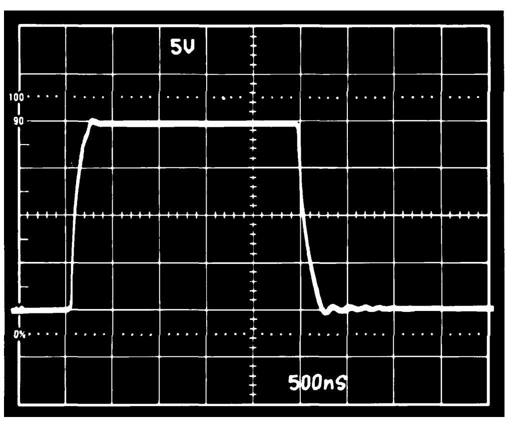


Figure 32. Driving 1000 pF C_L with Feed Forward Network of Figure 31

Settling Time

Settling time is measured with the circuit of Figure 33. This circuit employs a false summing node, clamped by the two Schottky diodes, to create the error signal and limit the input signal to the oscilloscope. For measuring settling time, the ratio of R6/R5 is equal to R1/R2. For unity gain, R6 = R5 = 1 kΩ, and R_L = 500 Ω. For the gain of –10, R5 = 50 Ω, R6 = 500 Ω and R_L was not used since the summing network loads the output with approximately 275 Ω. Using this network in a unity-gain configuration, settling time is 100 ns to 0.1% for a –5 V to +5 V step with C_L = 10 pF.

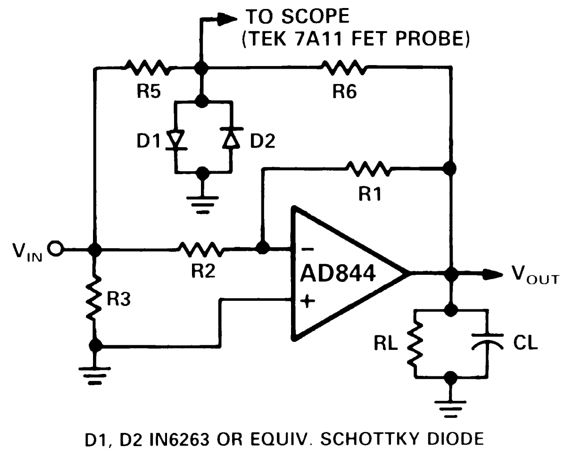


Figure 33. Settling Time Test Fixture

DC Error Calculation

Figure 34 shows a model of the dc error and noise sources for the AD844. The inverting input bias current, I_{BN}, flows in the feedback resistor. I_{BP}, the noninverting input bias current, flows in the resistance at Pin 3 (R_P), and the resulting voltage (plus any offset voltage) will appear at the inverting input. The total error, V_O, at the output is:

$$V_O = (I_{BP}\ R_P + V_{OS} + I_{BN}\ R_{IN})\left(1 + \frac{R1}{R2}\right) + I_{BN}\ R1$$

Since I_{BN} and I_{BP} are unrelated both in sign and magnitude, inserting a resistor in series with the noninverting input will not necessarily reduce dc error and may actually increase it.

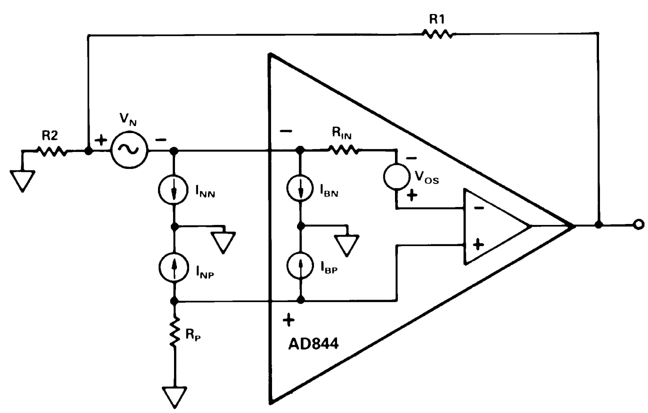


Figure 34. Offset Voltage and Noise Model for the AD844

Noise

Noise sources can be modeled in a manner similar to the dc bias currents, but the noise sources are Inn, Inp, Vn, and the amplifier induced noise at the output, V_{ON}, is:

$$V_{ON} = \sqrt{((Inp\ R_P)^2 + Vn^2)\left(1 + \frac{R1}{R2}\right)^2 + (Inn\ R1)^2}$$

Overall noise can be reduced by keeping all resistor values to a minimum. With typical numbers, R1 = R2 = 1k, R_P = 0, Vn = 2 nV/√Hz, Inp = 10 pA/√Hz, Inn = 12 pA/√Hz, V_{ON} calculates to 12 nV/√Hz. The current noise is dominant in this case, as it will be in most low gain applications.

Video Cable Driver Using ±5 Volt Supplies

The AD844 can be used to drive low impedance cables. Using ±5 V supplies, a 100 Ω load can be driven to ±2.5 V with low distortion. Figure 35a shows an illustrative application which provides a noninverting gain of 2, allowing the cable to be reverse-terminated while delivering an overall gain of +1 to the load. The –3 dB bandwidth of this circuit is typically 30 MHz. Figure 35b shows a differential gain and phase test setup. In video applications, differential-phase and differential-gain characteristics are often important. Figure 35c shows the variation in phase as the load voltage varies. Figure 35d shows the gain variation.

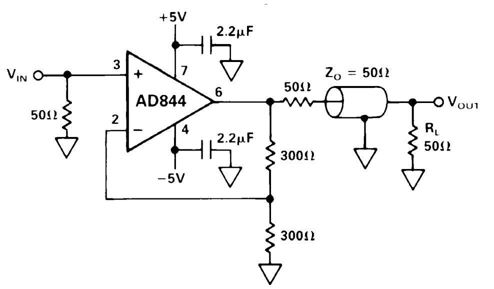


Figure 35a. The AD844 as a Cable Driver

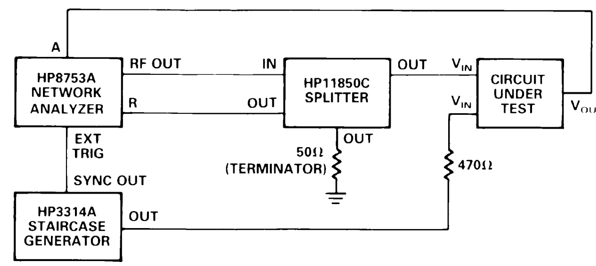


Figure 35b. Differential Gain/Phase Test Setup

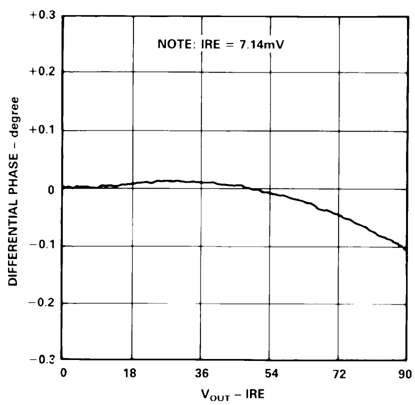


Figure 35c. Differential Phase for the Circuit of Figure 35a

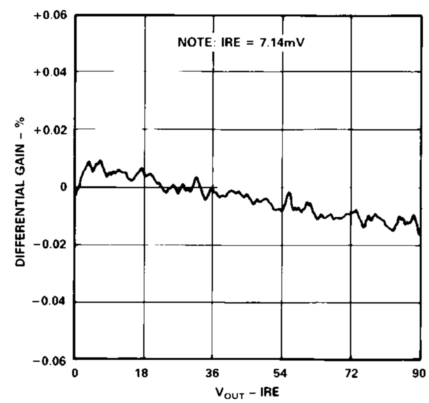


Figure 35d. Differential Gain for the Circuit of Figure 35a

High Speed DAC Buffer

The AD844 performs very well in applications requiring current-to-voltage conversion. Figure 36 shows connections for use with the AD568 current output DAC. In this application the bipolar offset is used so that the full-scale current is ±5.12 mA, which generates an output of ±5.12 V using the 1 kΩ application resistor on the AD568. Figure 37 shows the full-scale transient response. Care is needed in power supply decoupling and grounding techniques to achieve the full 12-bit accuracy and realize the fast settling capabilities of the system. The unmarked capacitors in this figure are 0.1 µF ceramic (for example, AVX Type SR305C104KAA), and the ferrite inductors should be about 2.5 µH (for example, Fair-Rite Type 2743002122). The AD568 data sheet should be consulted for more complete details about its use.

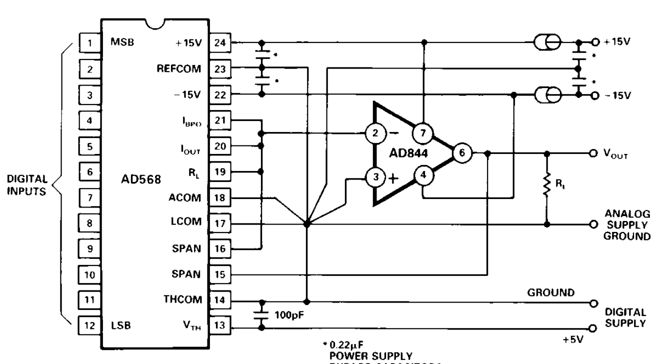


Figure 36. High Speed DAC Amplifier

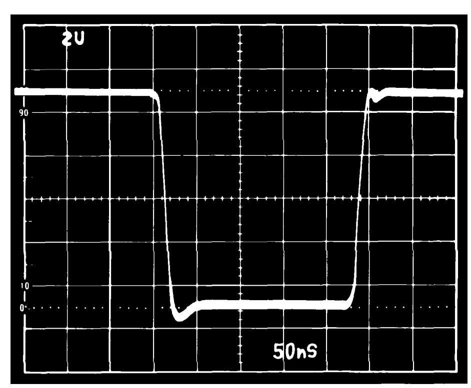


Figure 37. DAC Amplifier Full-Scale Transient Response

20 MHz Variable Gain Amplifier

The AD844 is an excellent choice as an output amplifier for the AD539 multiplier, in all of its connection modes. (See AD539 data sheet for full details.) Figure 38 shows a simple multiplier providing the output:

$$V_W = -\frac{V_X V_Y}{2V}$$

where V_X is the "gain control" input, a positive voltage of from 0 V to +3.2 V (max) and V_Y is the "signal voltage", nominally ±2 V FS but capable of operation up to ±4.2 V. The peak output in this configuration is thus ±6.7 V. Using all four of the internal application resistors provided on the AD539 in parallel results in a feedback resistance of 1.5 kΩ, at which value the bandwidth of the AD844 is about 22 MHz, and is essentially independent of V_X. The gain at V_X = 3.16 V is +4 dB.

Figure 39 shows the small signal response for a 50 dB gain control range (V_X = +10 mV to +3.16 V). At small values of V_X, capacitive feedthrough on the PC board becomes troublesome, and very careful layout techniques are needed to minimize this problem. A ground strip between the pins of the AD539 will be helpful in this regard. Figure 40 shows the response to a 2 V pulse on V_Y for V_X = +1 V, +2 V and +3 V. For these results, a load resistor of 500 Ω was used and the supplies were ±9 V. The multiplier will operate from supplies between ±4.5 V and ±16.5 V.

Disconnecting Pins 9 and 16 on the AD539 alters the denominator in the above expression to 1 V, and the bandwidth will be approximately 10 MHz, with a maximum gain of 10 dB. Using only Pin 9 or Pin 16 results in a denominator of 0.5 V, a bandwidth of 5 MHz and a maximum gain of 16 dB.

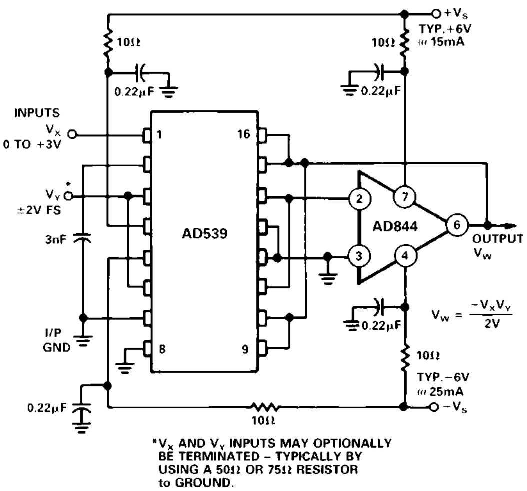


Figure 38. 20 MHz VGA Using the AD539

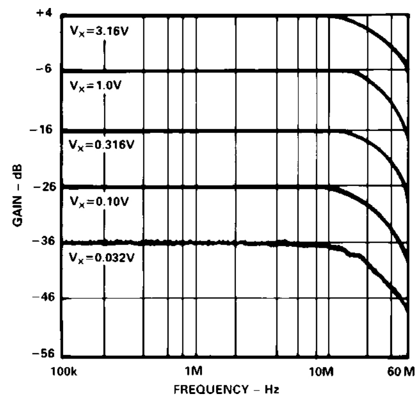


Figure 39. VGA AC Response

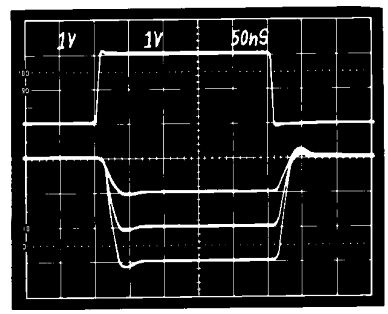
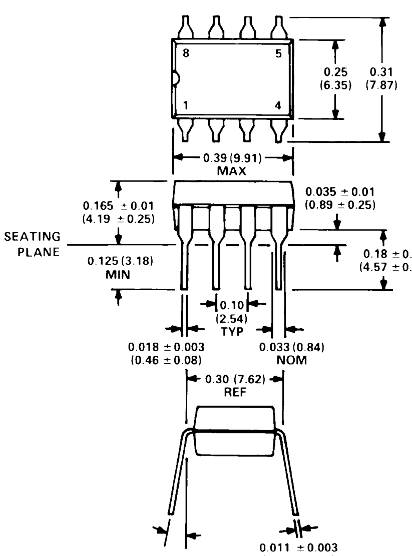


Figure 40. VGA Transient Response with V_X = 1 V, 2 V, and 3 V

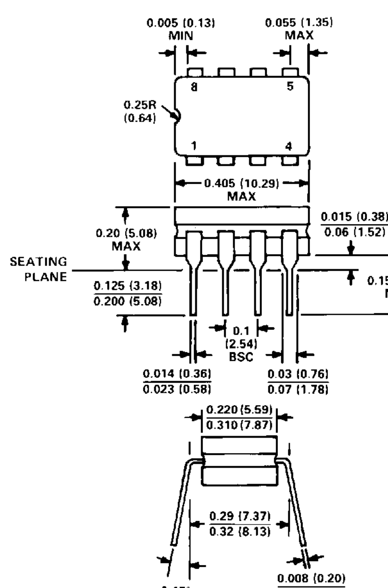
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

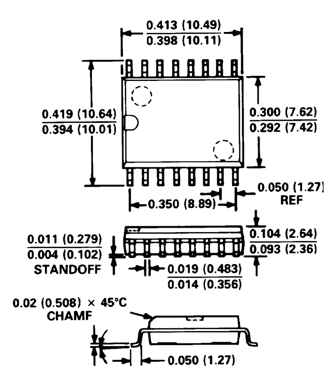
Mini-DIP (N) Package



Cerdip (Q) Package



16-Pin SOIC (R) Package



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